2.5.1 Reforms in Continuous Internal Evaluation(CIE) System at the Institution level

The institute believes firmly in continuous evaluation of the students for their sustained performance. As the institution is affiliated to JNTUK, Kakinada, exam and evaluation pattern given by the university is followed. As per the university regulations, 2 internal exams will be conducted which consists of descriptive and quiz exams. Out of these quiz will be the online exam conducted by the university. For lab courses also, internal exam will be conducted. Other than, these exams, for continuous evaluation of the students, unit tests and surprise tests will be conducted for the students. Continuous evaluation procedure is followed for practical subjects also. The department will carry out internal assessment on all subjects based on internal test performance of the students.

Effective implementation of evaluation reform of the university are strictly followed and those initiated by its own are ensured by the institution by strict compliance of process and procedure devised/ suggested by the university in order to follow the continuous evaluation system. The Institute has taken following measures for the effective implementation of the evaluation reforms introduced by the University: The Institute has exam coordinators from each department for smooth conduction of the examination. The examination committee meets periodically to discuss all the examination related matters. At Institute level, effective implementation of tutorial and mid exam takes place and results are declared within a week. The students can see their evaluated answer sheets and discuss the same with concerned faculty. Final year project work is jointly evaluated by external examiners. After releasing the semester examination results, the last date to apply for Revaluation/ Recounting/ Challenge Valuation will be informed by the university. Students can apply by their own through online.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA

EXAMINATION BRANCH, KAKINADA

III B TECH - II SEMESTER (R13 REGULATION) I MID EXAMINATIONS – JAN, 2018

T I M E T A B L E

BRANCH	DATE AND DAY						
	18-01-2018 (Thursday)	**19-01-2018 (Friday)**	**20-01-2018 (Saturday)**	**22-01-2018 (Monday)**	**24-01-2018 (Wednesday)**	**25.01.2018 (Thursday)**	**27.01.2018 (Saturday)**
CIVIL ENGINEERING (01- CE)	Environmental Engineering – I	Geotechnical Engineering – II	Design and Drawing of Steel Structures	Water Resources Engineering–I	Transportation Engineering – II	-----	**Open Elective**
ELECTRICAL AND ELECTRONICS ENGINEERING (02 - EEE)	Microprocessors & Microcontrollers	Switchgear and Protection	Utilization of Electrical Energy	Power System Analysis	Management Science (comm to EEE and CHEM)	Power Semiconductor Drives	-----
MECHANICAL ENGINEERING (03 - ME)	Operations Research	Interactive Computer Graphics	Design of Machine Members– II	Robotics	Heat Transfer	Industrial Engineering Management	**Departmental Elective**
ELECTRONICS & COMMUNICATIONS ENGINEERING (04 - ECE)	Microprocessors and Microcontrollers (Com to ECE,EIE and E.Comp.E)	Digital Signal Processing	Digital Communications	Microwave Engineering	-----	-----	**Open Elective**
COMPUTER SCIENCE ENGINEERING (05 - CSE)	Software Engineering	Data Ware Housing and Mining (Comm to CSE,IT)	Computer Networks (Comm to CSE,IT)	Design and Analysis of Algorithms (Comm to CSE,IT)	Web Technologies (Comm to CSE,IT)	-----	IPR and Patents (COMM TO CSE, IT, CHEM, PE)

RAMACHANDRA COLLEGE OF ENGINEERING

(Approved by AICTE, New Delhi, Affiliated to JNTUK: Kakinada)
NH-5 Bypass Road, Vatluru (V), ELURU – 534 007, A. P.

Circular

Ref: RCEE/Exam Cell/Mid-I Circular/2018 Date: 03.01.2018

Guidelines to the faculty members regarding Mid-I Examinations for II& IIIB.Tech(R16,R13) - II Semester

1. I MID for II& III B.Tech will be commenced from 18.01.2018.
2. Question paper for **MID – I (Descriptive)** should be submitted to the Principal on or before **06/01/2018.**
3. Three questions will be given in the question paper and the students have to answer **all questions without choice.**
4. After the evaluation the marks should be submitted to the exam cell within **Two days after completion of the exam.**

PRINCIPAL

Copy to: The Chairman, Secretary and Correspondent

HOD – CE	HOD – EEE	HOD – ME	HOD – ECE	HOD – CSE
HOD – S&H	HOD – MBA	HOD - IMPACT	Exams Section	TPO
AO	PD	Library	Transportation	

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AO	PD	Library	Transportation	

II B.Tech

PDC – , Mrity (ECE-C)

ECA – ,

EMWTL –

AC –

MS –

CS – 5/1/2018.

III B.Tech

MWE – ,

MPMC – (ECE-C)

DSP –

DC –

FNN –

RAMACHANDRA COLLEGE OF ENGINEERING: ELURU

CIRCULAR

Ref: JNTUK/MID-I EXAMS/2017 Date: 11-01-2018

The following is the schedule of II B. Tech - II Semester Quiz-I (ONLINE-I) & Mid-I (Subjective Test-I) Exams.

II B. Tech II Semester (Starts from 18.01.2018 to 25.01.2018)

Branch	QUIZ-I (ONLINE-I)
EEE-A	10.00 AM TO 12.30 AM
EEE-B	
MECH-A	
MECH-B	
ECE-A	
ECE-B	
CE	
ECE-C	
CSE-A	
CSE-B	

Branch	MID-I (Subject Test-I)	Room No.	H.T.NO	No of Strength
CE	03.00PM To 04.30 PM	B-208	16ME1A0101 to002017ME5A0120	50
		B-011	17ME5A0121 to 17ME5A01[illegible]	15
EEE		C-017	16ME1A0201 TO 16ME1A0228	24
		C-018	16ME1A0229 TO 17ME5A0214	24
		C-216	17ME5A0215 TO 17ME5A0236, 16ME1A0240 TO 16ME1A0259	24
		C-217	16ME1A0260 TO 17ME5A0221	24
		C-006	17ME5A0222 TO 17ME5A0238	14
MECH		C-017	15ME1A0379, 15ME1A03A8, 16ME1A0302 TO 16ME1A0329	24
		C-018	16ME1A0330 TO 16ME1A0362	24
		C-216	16ME1A0363 TO 16ME1A0384, 16ME1A0304, 16ME1A0313 TO 16ME1A0318, 16ME1A0332 TO 16ME1A0365	24
		C-217	16ME1A0369 TO 17ME5A0316	24
		C-006	17ME5A0317 TO 17ME5A0347	31
ECE		C-003	16ME1A0401 TO 17ME5A0404, 15ME1A04B5, 16ME1A0461 TO 16ME1A0469	72
		B-101	16ME1A0470 TO 16ME1A0494	24
		B-105	16ME1A0495 TO 16ME1A04B8	24
		B-108	16ME1A04B9 TO 17ME5A0408, 16ME1A04C1 TO 16ME1A04D9	24
		A-309	16ME1A04E0 TO 16ME1A04G5	24
		A-310	16ME1A04G6 TO 17ME5A0413	19
CSE		A-302	16ME1A0501 TO 17ME5A0504, 15ME1A0544, 16ME1A0561 TO 16ME1A0569	72
		A-309	16ME1A0570 TO 16ME1A0593	24
		A-310	16ME1A0594 TO 16ME1A05B7	24
		B-011	16ME1A05B8 TO 17ME5A0505	05

11/01/18

Exam Section In-Charge

Principal

Copy to:

Vice-Principal HOD-CE HOD – EEE HOD – ME

HOD – ECE HOD – CSE

All the HODs for circulation among the Staff, Students and Notice boards

Ramachandra College of Engineering: ELURU

II, III B.Tech II Semester (R16, R13) MID-I Examinations, Jan-2018

ECE

III-II Exam (11.00 to 12.30) (FN)
II-II Exam (3.00 to 04.30) (AN)

		18.01.2018 (Thu)		19.01.2018 (Fri)		20.01.2018 (Sat)		22.01.2018 (Mon)		24.01.2018 (Wen)		25.01.2018 (Thu)		27.01.2018 (Sat)		
		FN	AN	FN	AN	FN	AN	FN	AN	FN	AN	FN	AN	FN	AN	Signature
1	Sri D Venkanna Babu			√	√			√		√						
2	Sri M.Rama Krishna			√	√			√								
3	Sri D Rambabu		√		√		√		√		√		√		√	
4	Sri R Durga Prasad		√		√				√				√			
5	Sri RLR Lokesh Babu							√		√	√					
6	Sri A Rajesh Naidu						√				√					
7	Sri N Venu				√			√								
8	Sri N V D P Murthy			√	√	√				√				√		
9	Sri R Raghu Ram	√	√						√		√	√	√			
10	Mr J Prasanth Kumar		√					√					√			
11	Sri N Ramakrishna						√							√		
12	Sri D Sridhar	√	√		√		√	√		√	√	√	√		√	
13	Smt Y Lavanya	√			√	√			√		√	√		√		
14	Sri R Radha Krishna		√		√				√				√			
15	Sri M Ravi Kiran											√				
16	Sri CH Joji Babu			√		√								√		
17	MS P Bhagya Sri									√						
18	Smt Ch Naga Lakshmi		√				√			√			√		√	
19	Sri P Satish Babu	√			√	√		√		√		√				
20	Sri M Ravi		√						√				√			
21	Sri G Rajesh Babu				√				√	√						

HOD

Principal

RAMACHANDRA COLLEGE OF ENGINEERING: ELURU

ATTENDANCE STATEMENT of ECE-B Room No : B-108

II B.Tech II Semester (R16) MID-I & MID-II Examinations, January-2018

Sl. No.	H.T. No.	MID-I	MID-II	MID-I	MID-II
		18-Jan	19-03-2018	19-Jan	20-03-2018
		MS		PDC	
		Signature of the Student			
1	16ME1A04B8	N.S.Sindhu	N.S.Sindhu	N.S.Sindhu	N.S.Sindhu
2	16ME1A04C0	N.Karuna	N.Karuna	N.Karuna	N.Karuna
3	17ME5A0405	B.Pavan Kalyan	B.Pavan Kalyan	B.Pavan Kalyan	B.Pavan Kalyan
4	17ME5A0406	G.Yeswanth Kumar	G.Yeswanth Kumar	G.Yeswanth Kumar	G.Yeswanth Kumar
5	17ME5A0407	G.Murali Krishna	G.Vamsi Krishna	G.Murali Krishna	G.Murali Krishna
6	17ME5A0408	— AB —	— AB —	— AB —	— AB —
7	16ME1A04C1	N.Jagadeesh babu	N.Jagadeesh babu	N.Jagadeesh babu	N.Jagadeesh babu
8	16ME1A04C2	N.Mahesh babu	N.Mahesh babu	N.Mahesh babu	N.Mahesh babu
9	16ME1A04C3	P.Sai Pavan Reddy	P.Sai Pavan Reddy	P.Sai Pavan Reddy	P.Sai Pavan Reddy
10	16ME1A04C4	P.Teja Sai	P.Teja Sai	P.Teja Sai	P.Teja Sai
11	16ME1A04C5	P.Mahendra	← ABSENT →	P.Mahendra	← ABSENT →
12	16ME1A04C6	P.Shamkhasai	P.Shakhasai	P.Shanmukhasai	P.Shankhasai
13	16ME1A04C7	P.Gayathri	P.Gayathri	P.Gayathri	P.Gayathri
14	16ME1A04C8	P.Likath	P.Likhitha	P.Likitha	P.Likitha
15	16ME1A04C9	P.Rishitha	P.Rishitha	Rishitha.P	Rishitha.P
16	16ME1A04D0	P.Bhanu Anusha	P.Bhanu Anusha	P.Bhanu Anusha	P.Bhanu Anusha
17	16ME1A04D1	P.pavithra	P.Pavithra	P.Pavithra	P.Pavithra
18	16ME1A04D2	P.Durga Bhavani	P.Durga Bhavani	P.Durga Bhavani	P.Durga Bhavani
19	16ME1A04D3	P.Stella Bright	P.Stella Bright	P.Stella Bright	P.Stella Bright
20	16ME1A04D4	Dedeepya.P	Dedeepya.P	Dedeepya.P	Dedeepya.P
21	16ME1A04D5	P.Sai Tanuj	P.Sai Tanuj	P.Sai Tanuj	P.Sai Tanuj
22	16ME1A04D7	— AB —	P.Sai mounika	— AB —	P.Saimounika
23	16ME1A04D8	P.Satya Sai	P.SatyaSai	P.Satyasai	P.Satya Sai
24	16ME1A04D9	P.Pavan Sai	P.Pavan Sai	P.Pavan Sai	P.Pavan Sai

No.of Presents	22	22	22	22
No.of Absents	02	02	02	02
Signature of the Invigilators	19/3/18 (M.Ravi)	19/3/18 (P.Valli Ravi)	19/3/18	20/03 (M.Sarika)

RAMACHANDRA COLLEGE OF ENGINEERING

NAAC B++ Grade

(Approved by AICTE, New Delhi, Affiliated to JNTUK: Kakinada)
NH-5 Bypass Road, Vatluru (V), ELURU – 534 007, A. P.

III-I B.TECH II MID EXAMINATIONS

SUBJECT: **Computer Architecture and Organization** Duration: 90 Min

Date : 08-10-2018 DESCRIPTIVE (Format:9004/0) Branch: ECE

****

Answer All *Three* questions Marks:30

1)	Explain about PCI Bus?	Understanding	10	CO4
2)	*Explain any one method to handle multiple devices by using Hardware?*	Applying	10	CO5
3)	Distinguish between Hardwired and Micro programmed Control and Draw their block Diagrams?	Analyzing	10	CO6

INTERNAL ASSESSMENT BOOK

Name of the Student : Ch. Geetha Krishna Priyanka

Hall Ticket No : 16ME1A0429

Branch / Program : ECE. **Year/Sem :** III - I **Section:** A

Course/Subject with Code : CAO

Name of Faculty	MID-I							MID-II							Final Marks
	Date:- 6-8-18							Date:- 8-10-18							
	Descriptive				Quiz (10M)	Assig (5M)	Total	Descriptive				Quiz (10M)	Assig (5M)	Total	
	1	2	3	4				1	2	3	4				
Raghu Kumar	8	10	6		5	5	22	3	10	10		5	5	22	22
	24/30		12/15					23/30		12/15					
Signature Staff	Raghu							Raghu							
Invigilator Name+signature with date	6/8/18 Lavanya							K.Kiran 8/10/18							

RAMACHANDRA
COLLEGE OF ENGINEERING

(Approved by AICTE New Delhi, Affiliated to JNTUK: Kakinada)
NH-5 Bypass Road, Vatluru (V), Eluru-534 007, A.P

2 Ans:

Isolated I/O	Memory mapped I/O
1. Seperate address is given for I/O (input and output) and memory	1. Same address is given for both I/O (input and output unit) and memory
2. Seperate instructions is given to read and write of I/O input and output unit and memory	2. Same instructions is given to read and write for both the I/O (input and output unit) and memory
3. The I/O address is known as ports	3. Normal memory address is used.
4. More efficient due to more buses	4. lesser efficient due to single bus
5 Large in size due to number of buses	5. Small in size because of single bus.
6. It is a complex to seperate logic for I/O (input and output unit) and memory	6. It is a simpler logic the I/O (input and output unit) is
7 Limited instructions is given in this to I/O input and output unit they are IN, OUT, INS and OUTS	7 Any instruction is given to this memory
8. Efficient I/O operator is used	8. Inefficient I/O operator due to single bus

10

3.

Ans: Addressing modes:-

It is a sequential way in which the operand is taken from the register (or) memory is known as Addressing modes.

Effective Addressing Mode:-

It is a memory address of the operand which is obtained from the computation by dictating the addressing mode is known as effective addressing modes.

Types of Addressing Modes:-

1. Immediate Addressing mode
2. Register Addressing mode
3. Register Indirect Addressing mode
4. Direct Addressing mode
5. Indirect Addressing mode
6. Implied Addressing mode
7. Relative Addressing mode
8. Indexed Addressing mode
9. Base register Addressing mode
10. Auto incremented (or) Auto decremented addressing mode

1. Immediate Addressing Mode:-

→ In this addressing mode the operand value to the register is given immediately

Ex:- MOV #200, R1; // R1 ← 200

→ # represents the immediate addressing mode

→ The operand 200 is stored into register 'R'

2. Register Addressing Mode:-

In this addressing mode only one of the register is processed

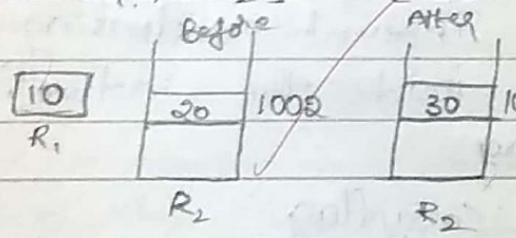
Ex:- Add R_1, R_2 // $R_2 \leftarrow R_1 + R_2$

→ The content of the register 'R_1' and 'R_2' are added and stored in register 'R_2'.

3. Register Indirect Addressing mode:-

→ In this addressing mode we use one register and another one is given as address of the register

Ex:- Add $R_1, [R_2]$ // $[R_2] \leftarrow R_1 + [R_2]$

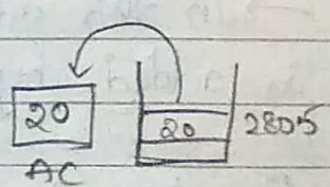


→ The content of R_1 and the value stored at the address of R_2 are added and stored into the address of R_2.

4. Direct Addressing mode:-

In this addressing mode we will take the accumulator

Ex:- LDA [2805H] // AC ← [2805]



where

LDA - LoaD Accumulator

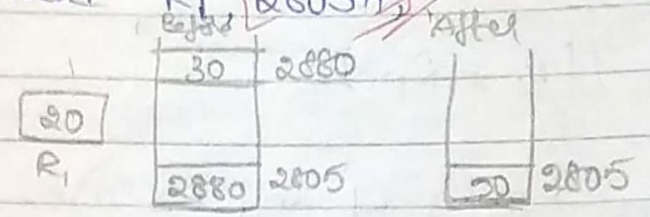
H - Hexadecimal format

→ the value (or) content in the address is stored into accumulator

5. Indirect Addressing Mode:-

→ In this addressing mode one is register and another one is Effective Address

Ex:- Add R1, [2805H];



→ The content of R1 and the memory address2 is memo. present in the another memory address1 the value in the memory address 2 are added and again stored in memory address 1 as shown above

6. Implied Addressing Mode:-

→ It is also known as Inherent addressing mode

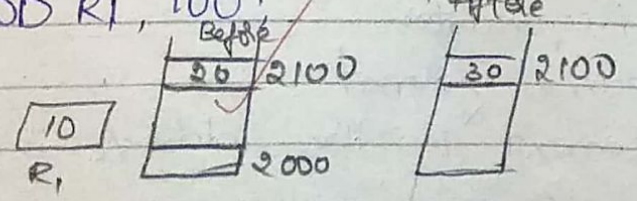
→ The operand is hidden inside the instructions

Ex:- STC // SeT Carryflag
CMC // CoMpliment Carryflag
CMA // CoMPliment Accumulator
CLA // CLear Accumulator

7. Relative Addressing mode:-

→ In this addressing mode the program counter value is added by given value in the instruction.

Ex:- ADD R1, 100;



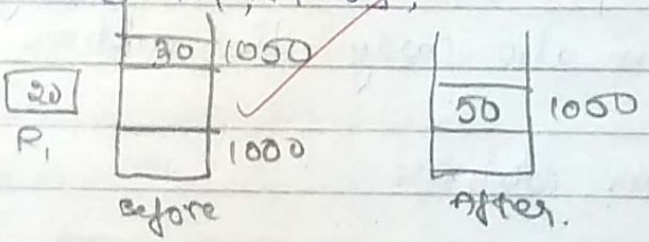
EA = content of PC + 100;

→ The content of register R_1 and the PC value is 2000 and in instruction 100 is given so 2000 + 100 = 2100 The value at the address 2100 is added and stored in the address 2100.

8. Indexed Addressing Mode :-

→ In this addressing mode the index[value] is given the index is incremented to that value

Ex :- ADD R_1, X[50];



EA = content of X + 50.

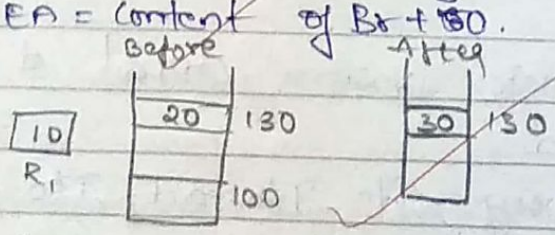
→ The content of register R_1 and the index value is 1000 and in instruction X[50] is given so i.e., 1000+50 1050. The value at that address is added and stored in the address 21050.

9. Base register Addressing mode :-

→ It is same as Indexed addressing mode

Ex :- ADD R1, Br[30];

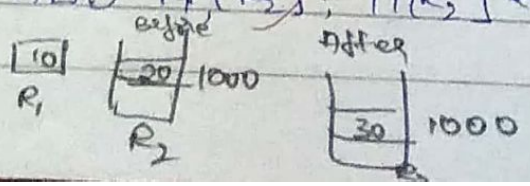
EA = Content of Br + 30.



10. Auto increment (or) Auto Decrement Addressing mode :-

It is same as the register Indirect Addressing mode in this it is auto increment (or) auto decrement to the memory

Ex :- ADD R_1[R_2]; // [R_2] ← R_1 + [R_2]



1Ans:- Bus structure :-

The computer is a collection of functional units. In-order to carry-out there process successfully the maintain exchange of information between each unit To exchange information functional units need certain interface. The transmitting medium with one (or) more wires can capable of exchanging data the bus is used

The bus carry the form signal to functional units. One signal per wire each wire carry one bit of data. The bus also carry the address and Control signals.

The system bus contains

1. Address bus
2. Data bus
3. Control bus.

1. Data bus :- It is a uni-directional bus. The data is transferred between system modules. It is a part of to overall performance.

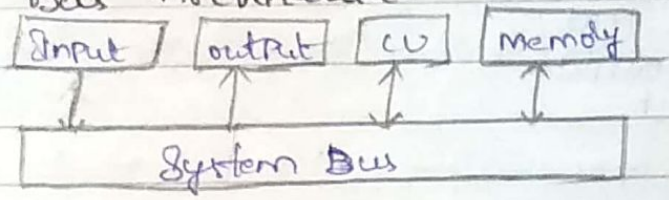
2. Address bus :- It is also a uni-directional bus. It gives the memory location of the address which is to be performed.

3. Control bus :- It carries various control & signal which are to be performed.

Ex:- Memory Read, Memory write, I/O read, I/O write.

In this Bus structure we have
1. Single bus Architecture
2. Traditional bus Architecture
3. High speed bus Architecture

1. Single bus Architecture:-



Advantage :- simple and less cost

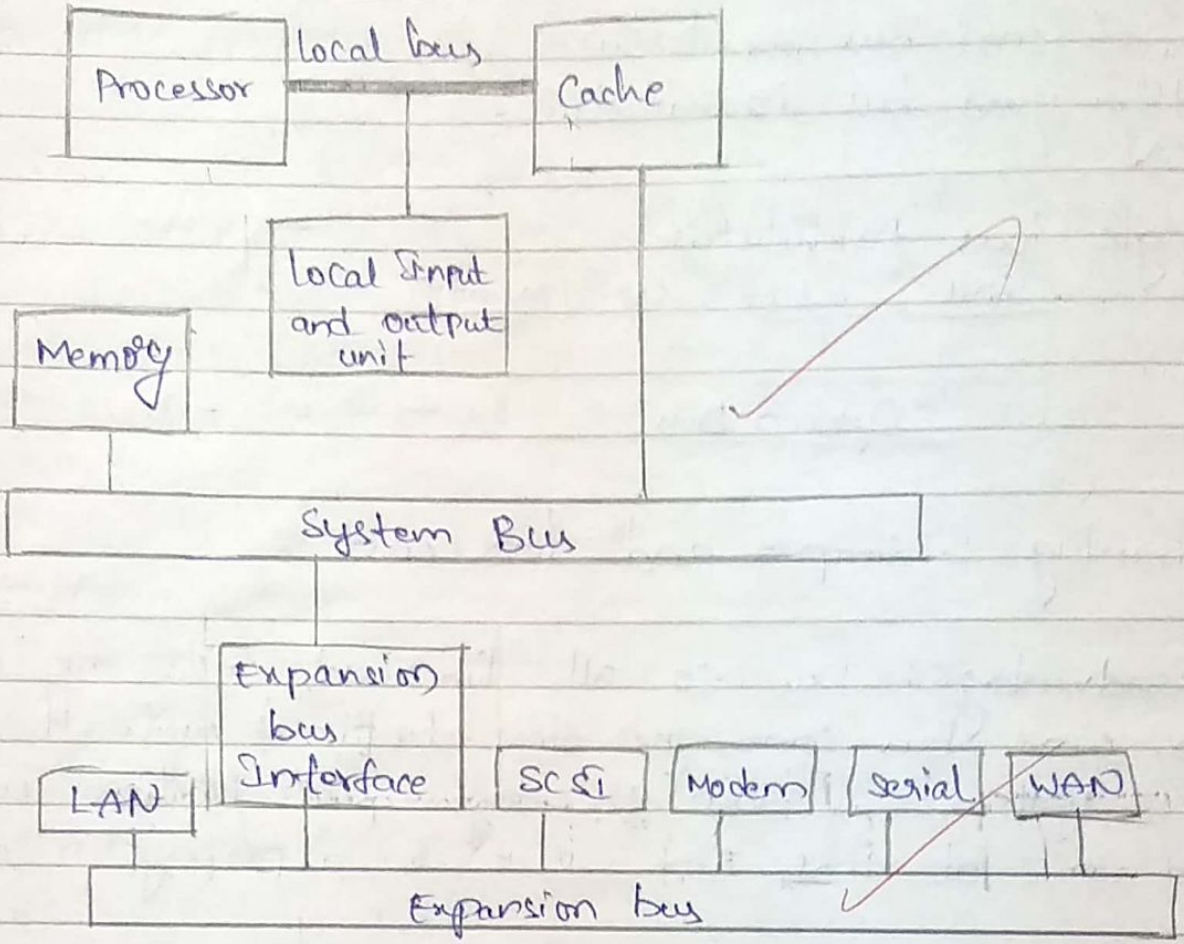
Disadvantage :- Due to all functional units are attached to same bus some are slow functional units if they use system bus then the high speed functional units can wait at that time so it is a propagation delay.

There are two drawbacks.

i) Because connecting all functional units to the same bus larger the size and propagation delay occurs.
ii) The it becomes the bottle neck the aggregate data is stored in that

To overcome these drawback we use.
1. Traditional bus architecture
2. High speed bus architecture.

1. Traditional Bus Architecture :-



Now-a-days In most of the computer systems these Traditional Bus Architecture is used.

The local bus is used to connect the processor and cache. The local bus is also connected to the local input and output unit. Cache not only connected to the local bus but also to the system bus.

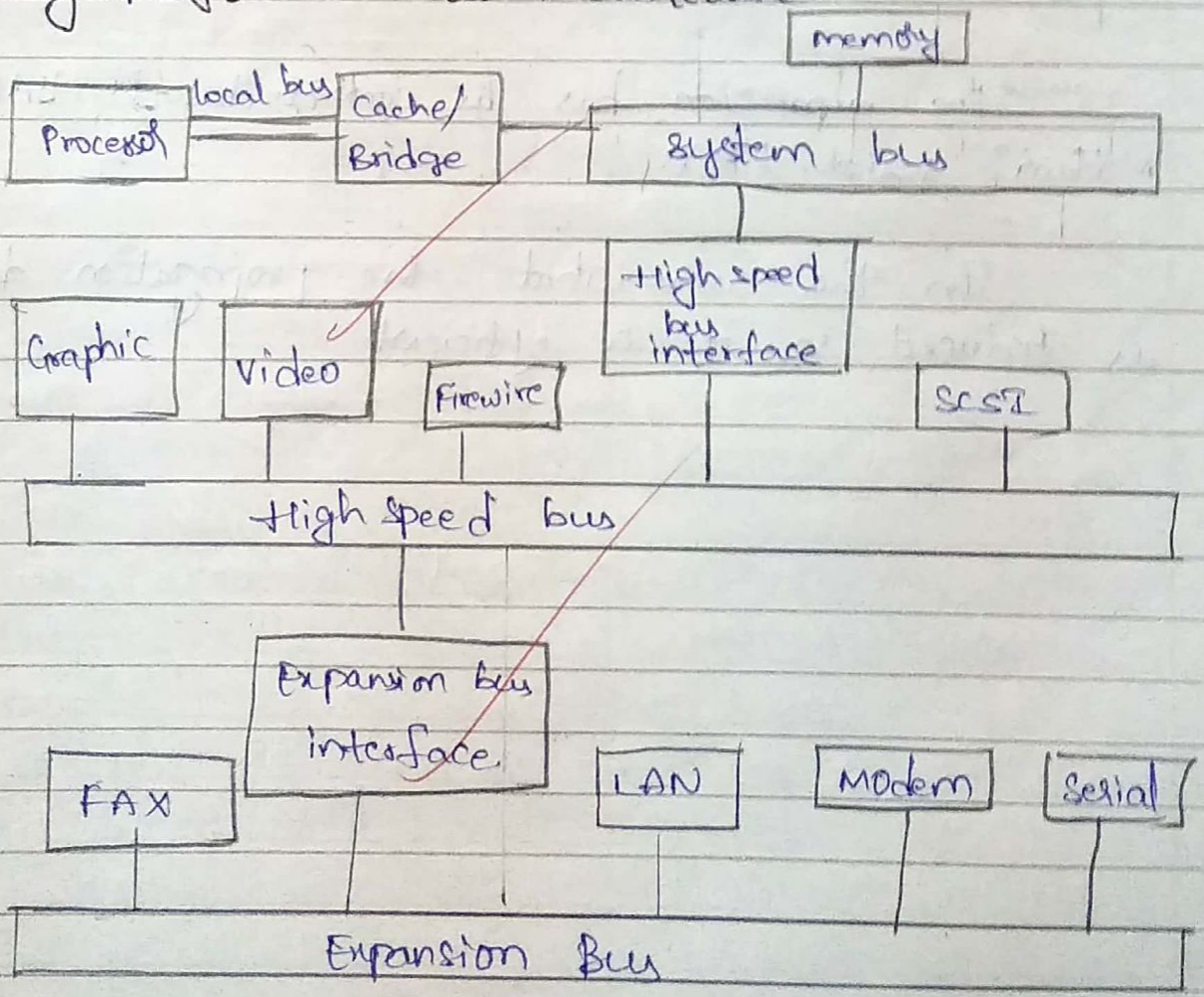
Due to this structure the processor not access the memory frequently. It uses cache and the processing is done. If any data memory is not present in the cache which is required for the processing then

the processor take that data from the main memory and stored it in cache to use next time.

So, the memory is moved off. So, the Expansion bus is use that main memory and access. The Expansion bus is connected with LAN, WAN, SCSI, Modem and serial etc., The Expansion bus interface is connected to the system bus.

But here also there is propagation delay because for the expansion bus all high speed and slow funtional units are connected.

2. High Peaforme Bus Architecture :-



In this high performance bus architecture the local bus is connected to processor and cache/Bridge that is connected to system Bus the system Bus is connected to main memory.

Here the slow speed functional units are connected to Expansion bus and high speed functional units are connects to the high speed bus.

For high speed bus the high speed functional units Graphic, Video, Firewire, SCSI etc are connected the high speed functional units is near to main memory so it access the memory and then the expansion bus functional units are used.

The expansion bus is connected with LAN, Modem, serial, FAX.

In this some-what the propagation delay is reduced so it is efficient

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An ISO 9001: 2015 certified & NAAC accredited Institution
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Department of Electronics and Communication Engineering

III-II B.TECH II MID EXAMINATIONS

SUBJECT: MPMC — Duration: 90 Min

Date : 25-03-2019 — DESCRIPTIVE (Format: 9004/0) — Branch: ECE- A , B & C

****

Answer All *Three* questions

		Marks	Cognitive level	CO
1)	Explain the Paging scheme of 80836 Microprocessor and scaled addressing modesof 80386 in detail.	10 M	Remembering	CO4
2)	Explain the architecture of 8051 microcontroller with a neat sketches.	10 M	Understanding	CO5
3)a	Explain the features of PIC microcontroller and give description about parallel ports available in PIC.	10 M	Understanding	CO6

Faculty
1) RVR 15/3
2)

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Subject Expert

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Branch / Program : ECE **Year/Sem :** III-II **Section:** B

Course/Subject with Code : MPMC

Name of Faculty	MID-I						MID-II						Final Marks
	Date:- 30/11/19						Date:- 25/3/19.						
	Descriptive				Quiz (10M)	Assig (5M)	Total	Descriptive				Quiz (10M)	Assig (5M)	Total	
	1	2	3	4				1	2	3	4				
Lokesh Sir	8	7	6		04	5	21/30	9	7	7		06	5	23	23
	23/12							23/12							
Signature Staff															
Invigilator Name+signature with date	MURAM 23/11/19							M.R.Sekhar 25/3/19							

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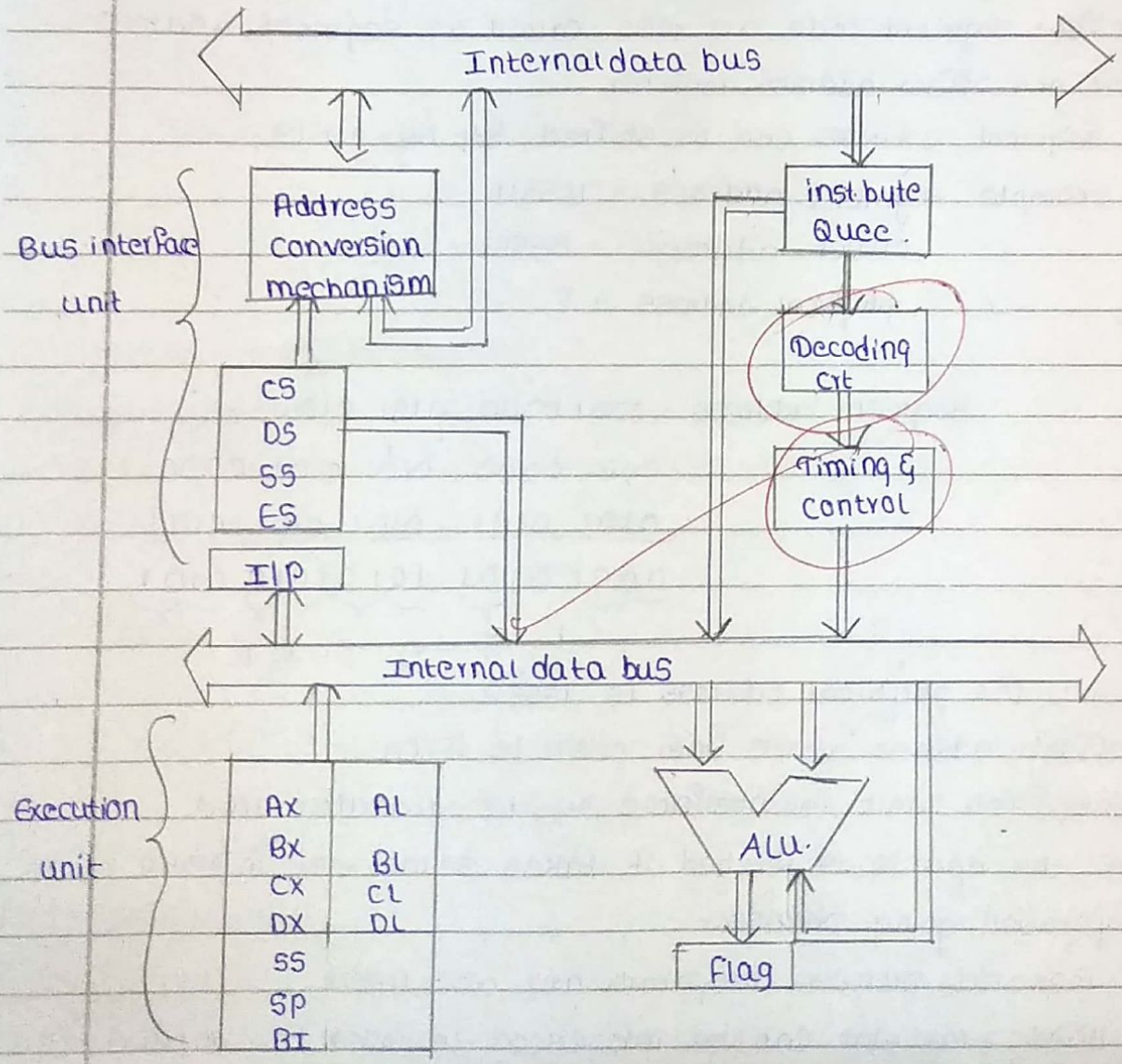
① Architecture of 8086 microprocessor :-

The architecture of 8086 consists of two units. they are
Bus interface unit
Execution unit.

Block diagram of 8086 architecture :-



The bus interface unit can perform the physical address calculations and predecoding of byte Quee. the bus interface unit control the system bus signals to provide effective address of the memory locations.

- It consists inorder to establish the communications of physical effective address.
- The physical address is combined by two address are given beloco
  (i) segment address
  (ii) offset address
- The physical address consists of a 20 Address bits long. and segment and offset contains 16 bits each.
- In offset, segment code are also called as segment address register and offset address register.
- The segment address can be shifted ~~left~~ by 4bits.
- for example segment address = 1055H
  offset address = 5555H
  physical address = ?

Segment address = 0001 0000 0101 0101

0001 0000 0101 0101 0000

0101 0101 0101 0101 0101

0001 0101 1010 1010 0101

1 5 5 5 A

∴ The physical address is 1555A.

- The offset address varies from 000H to FFFFH.
- Businterface unit is interfaced by the execution unit.
- when the opcode is fetched it takes some rest in 8259 even the operation going processor
- Here General purpose registers are also used.
  In 8086 time slot can be introduced in order to improve the timing signals.
- Ip :- Instruction pointer.
  which holds the addresses of the memory location.

• Decoding cir :-

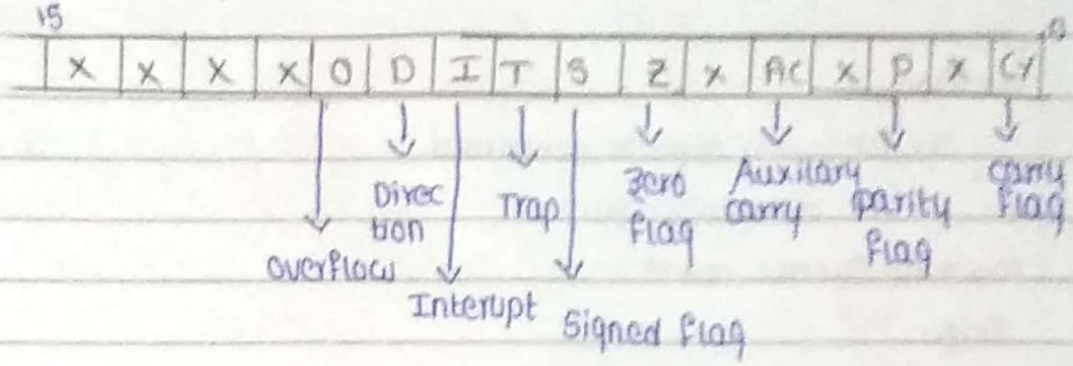
that instruction is used to decode the code operands.

• Timing and control cits :-

It requires to control the timing signals.

Flag register :-

it requires 16 bit flag registers



The flag registers are classified two modes.

1. conditional/status code
2. machine control codes

conditional/status code :-

it consists of 6 types. they are given beloco

carryflag :- when we perform arthematic operation carry is generated

CF=1

otherwise CF=0

parity flag :

AH	AL

The LSB consists odd value the parity flag exists.

The value contains even the parity flag not exit.

Auxilary carry :-

AH	AL	AH	AL

the lower nibble if carry is generated AF=1

otherwise =0

Zero flag :-

All the values contain zero then ZF=1

otherwise ZF=0

Signed flag :-

if is is in negative the signed flag exists

Overflow :-

Overflow=1 ⇒ carry is generated.

otherwise zero

Machine Control codes :

Trap :

Trap = 1; it executes step by step

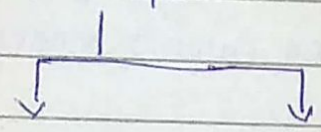
Trap = 0; Normal mode

Direction :

direction = 1 (Auto decrement)

direction = 0 (Auto increment)

interupt



IF=0 IF=1

(2) Instruction set of 8086 microprocessor :

There are 8 types of instruction sets

1. Data type/transfer instruction
2. Arthematic/logical instruction
3. loop instruction
4. Branch instruction
5. flag manipulation instruction
6. String instruction

7. Machine control instruction
8. shift / rotate instructions

Data type/ transfer instruction :-

The data is transfered from the source operand to desitination operation MOV, XCHG, I/O instructions belongs to this category.

MOV :-

The data is transfered from specified memory locations (source) and (destination)

```
Ex :- MOV DS, 5000H;
      MOV AX, BX;
      MOV AX, [SI];
```

XCHG :-

This instruction is used to exchange the data from the specified memory locations.

```
Ex :- MOV 5000H, DS;
      MOV BX, AX;
      MOV [SI], AX;
```

Arthematic/ logical instruction :-

This instruction performs arthematic, and logical operations. increment, decrement, compare, scan belongs to this categeory.

ADD :-

This instruction is added the data in the particular memory locations

```
Ex :- ADD
      ~~MOV~~ AX, BX ;
      ADD
      ~~MOV~~ AX [SI];
```

ADC :- ADD with carry.

This instruction performs the same addition process but carry is generated.

```
ADC AX, BX ;
ADC AX [SI];
```

Subtract :-

The data is subtracted the source operend from the destination operend and result is stored in the destination index

Eg :- SUB AX, BX

SUB AX [500H]

logical instructions :- These are used to perform NAND, NOR, OR logical operations. NAND, OR, NOT are the logical instructions.

AH 04H => 0000 0100

AL 01H 0000 0001

0000 0000

00

OR Gate :-

AH 05H => 0000 0101

AL 03H 0000 0110

0000 0111

07H

Branch instruction :-

This instruction transfer the control of the executed specified address it can be classified into two types.

(i) unconditional

(ii) conditional

unconditional :-

CALL :- instruction is used to call the sub routine program to another program

RET :- Return within segment

Return segment.

Conditional :-

JZ/JE : Jump on equal/Jump on zero

JNZ/JNE : Jump not equal

Shift rotate instruction : These are used to shift/rotateed by bit to bit wise.

SAR - shift arthematic Right

SHR - shift logical right

ROR - Rotate Right logical

ROL : Rotate left logical

Machine control instruction :-

This instruction is used to machine with status.

WAIT, NOP etc - - -

Flag instruction : In this instruction all the flag registers are effected directly.

CLC : clear carry flag

CLD : Clear direction flag

STD : Set direction flag

STC : set carry flag

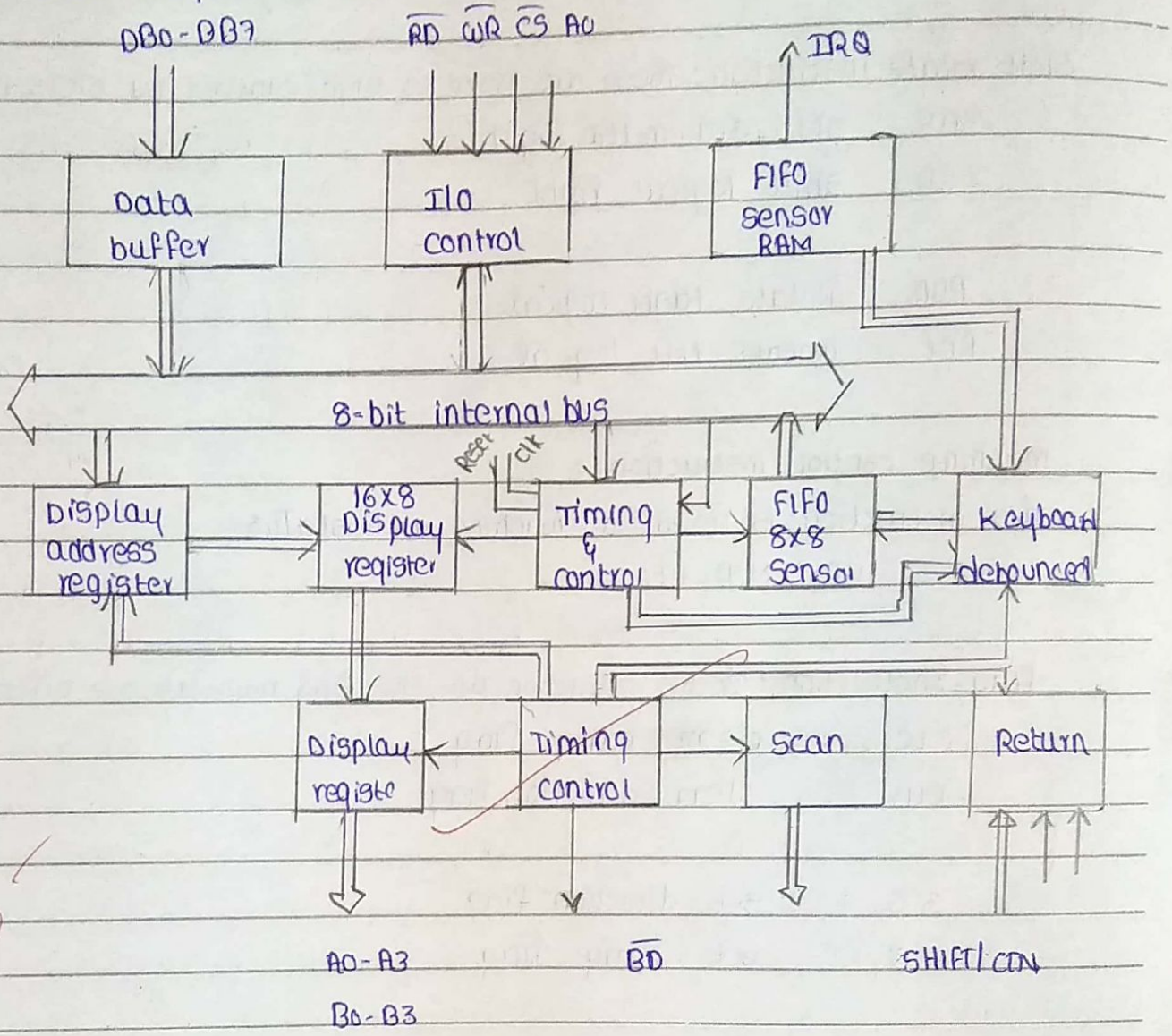
String instruction : These instruction are used to perform string manipulations

MOVS : moving into string.

MOSB : moving string on byte length

MOWS : moving string on word length

3 8279 :- keyboard control / display mode. it consists 40 pins description. The block diagram of the 8279 is



Here 8279 consists four selection lines and eight return lines and eight output lines. it consists two types of modes keyboard control mode display control mode

Data buffer :- it is used to transfer the data. I/O operations are enabled when $\overline{D}$ is low. remaining $\overline{RD}$, $\overline{WR}$ A0 are the operations performed by the cpu. it is used to store the keyboard/display in this mode

FIFO sensor :-

First - in - first out. it is related to stack point. it is decremented by 2.

Scan :-

it can be divided into two parts. key shift matrix and to display in encoded mode the operation executed externally. in decoded mode it exists internally.

Timing & control crl :-

It is used to control the timing signal in the operation.

Keyboard/debounced :-

when we hold the key it goes to debounced. the key is holded by sometime it is detected.

Display address register :-

In this it holds the address to be executed. it is automatically updated in 8279